WHAT IS CLAIMED IS:

1. A method of transferring data from circuitry disposed in a higher frequency clock domain to circuitry disposed in a lower frequency clock domain, said higher frequency clock domain operating with a first clock signal and said lower frequency clock domain operating with a second clock signal, comprising the steps:

latching said data in a first latch to generate a first latched data output, said first latch operating in response to a first modified clock signal that is synthesized at least in part from said first clock signal;

providing said first latched data output to a second latch disposed in said lower frequency clock domain, wherein said second latch is gated by a second modified clock signal synthesized at least in part from said second clock signal, said second latch operating to generate a second latched data output; and

providing said second latched data output to a register clocked by said second clock signal for generating a synchronized data output operable to be supplied to said circuitry disposed in said lower frequency clock domain.

2. The method of transferring data as set forth in claim 1, wherein said first and second clock signals are provided at a ratio of [N:M], where N equals the number of cycles of said first clock signal and M equals the number of cycles of said second clock signal and further equals (N-1), said cycles of said first and second clock signals being disposed between two substantially coincident rising edges of said first and second clocks signals that demarcate a coincident edge (CE) interval.

3. The method of transferring data as set forth in claim 2, wherein said first modified clock signal is manufactured from a plurality of intermediary clock signals that are generated in a particular relationship to said first clock signal and said second modified clock signal is manufactured from at least one intermediary clock signal that is generated in a particular relationship to said second clock signal.

4. The method of transferring data as set forth in claim 3, wherein said plurality of intermediary clock signals that are generated in a particular relationship to said first clock signal comprise CHOP_CORE1, CHOP_CORE2 and CHOP_CORE3 signals and said at least one intermediary clock signal that is generated in a particular relationship to said second clock signal comprises a CHOP_BUS signal.

5. The method of transferring data as set forth in claim 3, wherein said CHOP_CORE1 signal is generated such that its rising edge is triggered based on an (N-2)th rising edge of said first clock signal in a particular CE interval and its falling edge is triggered based on an (N-2)th falling edge of said first clock signal in said particular CE interval.

6. The method of transferring data as set forth in claim 5, wherein said CHOP_CORE2 signal is generated such that its rising edge is triggered based on an (N-1)th rising edge of said first clock signal in said particular CE interval and its falling edge is triggered based on an Nth rising edge of said first clock signal in said particular CE interval.

7. The method of transferring data as set forth in claim 6, wherein said CHOP_CORE3 signal is generated such that its falling edge is triggered based on said Nth rising edge of said first clock signal in said particular CE interval and its rising edge is triggered based on an Nth falling edge of said first clock signal in said particular CE interval.

8. The method of transferring data as set forth in claim 7, wherein said CHOP_BUS signal is generated such that its falling edge is triggered based on an (M-2)th falling edge of said second clock signal in said particular CE interval and its rising edge is triggered based on an (M-1)th falling edge of said second clock signal in said particular CE interval.

9. The method of transferring data as set forth in claim 8, wherein said rising edge of said CHOP_CORE1 signal is delayed by a propagation delay of approximately about 800 picoseconds from said (N-2)th rising edge of said first clock signal in said particular CE interval.

10. The method of transferring data as set forth in claim 9, wherein said falling edge of said CHOP_CORE1 signal is delayed by a propagation delay of approximately about 800 picoseconds from said (N-2)th rising edge of said first clock signal in said particular CE interval.

11. The method of transferring data as set forth in claim 8, wherein said rising edge of said CHOP_CORE2 signal is delayed by a propagation delay of approximately about 400 picoseconds from said (N-1)th rising edge of said first clock signal in said particular CE interval.

12. The method of transferring data as set forth in claim 11, wherein said falling edge of said CHOP_CORE2 signal is delayed by a propagation delay of approximately about 400 picoseconds from said Nth rising edge of said first clock signal in said particular CE interval.

13. The method of transferring data as set forth in claim 8, wherein said falling edge of said CHOP_CORE3 signal is delayed by a propagation delay of approximately about 400 picoseconds from said Nth rising edge of said first clock signal in said particular CE interval.

14. The method of transferring data as set forth in claim 13, wherein said rising edge of said CHOP_CORE3 signal is delayed by a propagation delay of approximately about 400 picoseconds from said second Nth falling edge of said first clock signal in said particular CE interval.

15. The method of transferring data as set forth in claim 8, wherein said falling edge of said CHOP_BUS signal is delayed by a propagation delay of approximately about 400 picoseconds from said (M-2)th falling edge of said second clock signal in said particular CE interval.

16. The method of transferring data as set forth in claim 15, wherein said rising edge of said CHOP_BUS signal is delayed by a propagation delay of approximately about 400 picoseconds from said (M-1)th falling edge of said second clock signal in said particular CE interval.

17. The method of transferring data as set forth in claim 4, wherein said first modified clock signal is manufactured by a logic circuit disposed in said higher frequency clock domain, said logic circuit comprising an OR gate for ORing said CHOP_CORE1, CHOP_CORE2 and first clock signals and an AND gate operable to accept said CHOP_CORE3 signal for ANDing with an output generated by said OR gate.

18. The method of transferring data as set forth in claim 4, wherein said second modified clock signal is manufactured by a logic circuit disposed in said lower frequency clock domain, said logic circuit comprising an AND gate operable to accept said CHOP_BUS signal for ANDing with said second clock signal.

19. A method of transferring data across a clock domain boundary, comprising the steps:

latching data provided by circuitry disposed in a first frequency domain to generate a first latched data output, said latching step being gated in conjunction with a first modified clock signal that is synthesized based on a first clock signal and three intermediary clock signals derived therefrom, wherein said first frequency domain is actuated by said first clock signal;

providing said first latched data output to a second latch disposed in a second frequency domain to generate a second latched output, said second latch being gated by a second modified clock signal that is synthesized based on a second clock signal and at least one intermediary clock signal derived therefrom, wherein said second frequency domain is actuated by said second clock signal;

providing said second latched data output to a register clocked by said second clock signal, said second register operating to generate a synchronized data output; and

providing said synchronized data output to circuitry disposed in said second frequency domain actuated by said second clock signal,

wherein said first clock signal operates at a higher frequency and said second clock signal operates at a lower frequency, said higher and lower frequencies being related in a ratio of [N:M], where N equals the number of cycles of said first clock signal and M equals the number of cycles of said second clock signal and further equals (N-1), said cycles of said first and second clock signals being disposed between two substantially coincident rising edges of

said first and second clocks signals that demarcate a coincident edge (CE) interval.

20. The method of transferring data across a clock domain boundary as set forth in claim 19, wherein first frequency domain is a core clock domain in a computer system.

21. The method of transferring data across a clock domain boundary as set forth in claim 20, wherein second frequency domain is a bus clock domain in a computer system.

22. The method of transferring data across a clock domain boundary as set forth in claim 19, wherein a first intermediary clock signal derived from said first clock signal is generated such that its rising edge is triggered with a propagation delay of about 800 picoseconds from an (N-2)th rising edge of said first clock signal in a particular CE interval and its falling edge is triggered with a propagation delay of about 800 picoseconds from an (N-2)th falling edge of said first clock signal in said particular CE interval.

23. The method of transferring data across a clock domain boundary as set forth in claim 19, wherein a second intermediary clock signal derived from said first clock signal is generated such that its rising edge is triggered with a propagation delay of about 400 picoseconds from an (N-1)th rising edge of said first clock signal in a particular CE interval and its falling edge is triggered with a propagation delay of about 400 picoseconds from an Nth rising edge of said first clock signal in said particular CE interval.

24. The method of transferring data across a clock domain boundary as set forth in claim 19, wherein a third intermediary clock signal derived from said first clock signal is generated such that its falling edge is triggered with a propagation delay of about 400 picoseconds from an Nth rising edge of said first clock signal in a particular CE interval and its rising edge is triggered with a propagation delay of about 400 picoseconds from an Nth falling edge of said first clock signal in said particular CE interval.

25. The method of transferring data across a clock domain boundary as set forth in claim 19, wherein said at least one intermediary clock signal derived from said second clock signal is generated such that its falling edge is triggered with a propagation delay of about 400 picoseconds from an (M-2)th falling edge of said second clock signal in a particular CE interval and its rising edge is triggered with a propagation delay of about 400 picoseconds from an (M-1)the falling edge of said second clock signal in said particular CE interval.

26. A system for transferring data from circuitry disposed in a first clock domain to circuitry disposed in a second clock domain, said first clock domain operating with a first clock signal and said second clock domain operating with a second clock signal, comprising:

a first latch gated by a first modified clock signal that is synthesized at least in part from said first clock signal, said first latch operating to generate a first latched data output based on data from said circuitry disposed in said first clock domain;

a first logic circuit operable to generate said first modified clock signal based on said first clock signal and a plurality of intermediary clock signals derived from said first clock signal;

a second latch disposed in said second clock domain, wherein said second latch is gated by a second modified clock signal synthesized at least in part from said second clock signal, said second latch operating to generate a second latched data output based on said first latched output received from said ;

a second logic circuit operable to generate said second modified clock signal based on said second clock signal and at least one intermediary clock signal derived from said second clock signal; and

a register clocked by said second clock signal for generating a synchronized data output upon receiving said second latched data output, said register operating responsive to said second clock signal to provide said synchronized data output to said circuitry disposed in said second clock domain.

27. The system for transferring data as set forth in claim 26, wherein said first and second clock signals are provided at a ratio of [N:M], where N equals the number of cycles of said first clock signal and M equals the number of cycles of said second clock signal and further equals (N-1), said cycles of said first and second clock signals being disposed between two substantially coincident rising edges of said first and second clocks signals that demarcate a coincident edge (CE) interval.

28. The system for transferring data as set forth in claim 27, wherein said intermediary clock signals derived from said first clock signal comprise CHOP_CORE1, CHOP_CORE2 and CHOP_CORE3 signals, each of which signals is generated in a particular relationship with respect to said first clock signal.

29. The system for transferring data as set forth in claim 28, wherein said at least one intermediary clock signal derived from said second clock signal comprises a CHOP_BUS signal that is generated in a particular relationship with respect to said first clock signal.

30. The system for transferring data as set forth in claim 29, wherein said first logic circuit comprises an OR gate for ORing said CHOP_CORE1, CHOP_CORE2 and first clock signals and an AND gate operable to accept said CHOP_CORE3 signal for ANDing with an output generated by said OR gate.

31. The system for transferring data as set forth in claim 29, wherein said second logic circuit comprises an AND gate operable to accept said CHOP_BUS signal for ANDing with said second clock signal.

32. The system for transferring data as set forth in claim 29, wherein said CHOP_CORE1 signal derived from said first clock signal is generated such that its rising edge is triggered with a propagation delay of about 800 picoseconds from an (N-2)th rising edge of said first clock signal in a particular CE interval and its falling edge is triggered with a propagation delay of about 800 picoseconds from an (N-2)th falling edge of said first clock signal in said particular CE interval.

33. The system for transferring data as set forth in claim 29, wherein said CHOP_CORE2 signal derived from said first clock signal is generated such that its rising edge is triggered with a propagation delay of about 400 picoseconds from an (N-1)th rising edge of said first clock signal in a particular CE interval and its falling edge is triggered with a propagation delay of about 400 picoseconds from an Nth rising edge of said first clock signal in said particular CE interval.

34. The system for transferring data as set forth in claim 29, wherein said CHOP_CORE3 signal derived from said first clock signal is generated such that its falling edge is triggered with a propagation delay of about 400 picoseconds from an Nth rising edge of said first clock signal in a particular CE interval and its rising edge is triggered with a propagation delay of about 400 picoseconds from an Nth falling edge of said first clock signal in said particular CE interval.

35. The system for transferring data as set forth in claim 29, wherein said CHOP_BUS signal derived from said second clock signal is generated such that its falling edge is triggered with a propagation delay of about 400 picoseconds from an (M-2)th falling edge of said second clock signal in a particular CE interval and its rising edge is triggered with a propagation delay of about 400 picoseconds from an (M-1)the falling edge of said second clock signal in said particular CE interval.

36. The system for transferring data as set forth in claim 29, wherein said first and second clocks are provided at a ratio of [1:1], and further wherein said intermediary clock signals comprise CHOP_CORE1, CHOP_CORE2 and CHOP_CORE3 and signals such that CHOP_CORE1 = CHOP_CORE2 = 0 and CHOP_CORE3 = 1, said CHOP_BUS being equal to 1.